REMARKS

This application has been amended so as to place it in condition for allowance at the time of the next Official Action.

The Official Action rejects claims 1, 2, 6, 7, 10, 11, 15 and 16 under 35 USC §102(b) as being anticipated by KAGEYAMA et al. 4,110,558. Reconsideration and withdrawal of this rejection are respectfully requested for the following reasons:

The Official Action identifies those components of the KAGEYAMA et al. device construed as meeting various elements recited in the rejected claims. These components of the KAGEYAMA et al. device include a parallel-in serial-out shift register, as well as structure to generate and verify check bits.

However, the nature of the KAGEYAMA et al. device is such that the parallel-serial translation in each case takes place in a single step, *i.e.*, serial data is converted into parallel data of its ultimate width in a single step, and vice versa.

The present invention takes a significantly different approach, as is evident from the description of the operation of the present invention beginning on page 8, line 4, with reference to Figure 2.

As is described therein, data being transferred from the parallel bus 1 to the serial bus 5 first passes through the parallel bus interface circuit 2. The parallel bus interface circuit receives the parallel data in its full width, e.g., 32

bits. The parallel bus interface circuit then multiplexes the full width data and sends it along the bus 9a to the parallel-serial interface circuit 3. This multiplexing may, *e.g.*, multiplex the 32-bit data into 8-bit bytes. The parallel-serial interface circuit 3 then generates and adds to each 8-bit data segment an error correcting code, and sends the combination to the parallel-serial converting circuit 4. The converting circuit 4 then sends the parallel 8-bit plus error correcting code parallel data into serial form and transmits it along the serial bus 5.

The transfer of serial data from the serial bus 5 to the parallel bus 1 essentially follows a largely parallel and corresponding path. The serial-parallel converting circuit takes the serial data with the error correcting code included therein and converts it into parallel data, received by the serial-parallel interface circuit 7. The interface circuit 7 checks the error correcting code against the parallel data to identify the existence of any transmission errors. The serial-parallel interface circuit 7 then sends each data segment which, as used in this example, is 8 bits wide to the parallel bus interface circuit 2. The interface circuit 2 then demultiplexes the 8-bit wide parallel data into 32-bit wide parallel data on the parallel bus 1.

As is evident from these characteristics of the present invention, conversion between full width parallel data and serial

data is incremental with the data taking an intermediate parallel form having a width less than that of the full width parallel data. Moreover, the error code generation and detection takes place on the reduced width intermediate form of the parallel data.

In order to highlight the differences between the present invention and the disclosure of the KAGEYAMA et al. reference, applicant has amended each of the independent claims to recite additional characteristics that represent the nature of the present device as utilizing an intermediate, narrow width parallel bus. As the KAGEYAMA et al. reference clearly fails to disclose such an arrangement, applicant respectfully suggests that the present anticipation rejection should be withdrawn.

The Official Action rejects claims 3-5 and 12-14 under 35 USC §102(b) as being anticipated by GOTZE et al. 4,450,561. Reconsideration and withdrawal of this rejection are respectfully requested for the following reasons:

The GOTZE et al. reference, like the KAGEYAMA et al. reference considered above, includes the conversion of data from serial to parallel form, as well as the use of error correction code (ECC) to allow single bit error correction and double bit error detection. However, like the KAGEYAMA et al. reference, the GOTZE et al. patent fails to disclose an arrangement that performs the translation between parallel and serial data using an intermediate, narrow width parallel bus. Therefore, for the

same reasons identified above, applicant respectfully suggests that the present anticipation rejection should be withdrawn.

The Official Action rejects claims 1, 6, 8-10, 15, 17 and 18 under 35 USC §103(a) as being unpatentable over GOTZE et al. and further in view of CARLTON et al. 4,218,742.

As discussed above in connection with the anticipation rejections, applicant has amended each of the independent claims to recite structure elements and method steps that define an interface between a parallel and serial bus that utilizes a narrow width parallel bus and the multiplexing and demultiplexing associated therewith. Neither the GOTZE et al. reference nor the CARLTON et al. reference, considered either individually or collectively, teaches such an arrangement, and reconsideration and withdrawal of the obviousness rejection are therefore respectfully requested.

In addition to the amendments described above, applicant has added new claims 19-26. Of these, claims 19-24 each recites that m = 32 and n = 8. Claims 25 and 26 depend from device claim 6 and method claim 15, respectively, and recite features related to the fact that data traveling along 9a from the parallel bus interface circuit follows a path different from data traveling along 9b to the parallel bus interface circuit, as illustrated in present Figure 2.

These features are similarly undisclosed by the known prior art, including the applied references.

Applicants have also amended the drawing sheet that includes FIG. 2. Element 3, which originally included the text "PARALLEL-SERIAL INTERFACE CIRCUIT" now additionally includes the text "(including check bit producer)". Element 7, which originally included the text "SERIAL-PARALLEL INTERFACE CIRCUIT" now additionally includes the text "(including error detector)". These specified additions of text are the only changes made to the identified drawing sheet. This addition does not amount to the addition of new matter, as "a check bit producer" and "an error detector" were disclosed in the application as originally filed in at least claims 1, 3-6, 8, 9, and 25, but not illustrated in Figure 2.

In light of the amendments provided above and the arguments offered in support thereof, applicant suggests that the present application is in condition for allowance, and an early indication of the same is respectfully requested.

If the Examiner has any questions or requires clarification of any of the above points, the Examiner is to contact the undersigned attorney so that this application may continue to be expeditiously advanced.

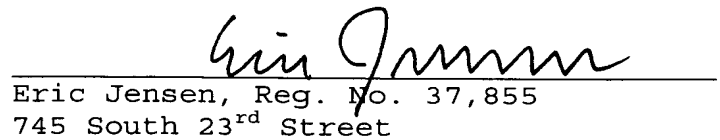
Please charge the fee of $100 for the two extra claims of any type added herewith to Deposit Account No. 25-0120.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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APPENDIX:

The Appendix includes the following item:

- replacement drawing sheet for Figure 2

AMENDMENTS TO THE DRAWINGS:

The attached sheet of drawings includes changes to Figure 2. This sheet, which includes Figure 2, replaces the original sheet including Figure 2. In Figure 2, element 3, which originally included the text "PARALLEL-SERIAL INTERFACE CIRCUIT" now additionally includes the text "(including check bit producer)". Element 7, which originally included the text "SERIAL-PARALLEL INTERFACE CIRCUIT" now additionally includes the text "(including error detector)".